L Number	Hits	Search Text	DB	Time stamp
1	872	"hardware accelerator"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 19:38
2	169	"hardware accelerator" and java	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 19:38
3	4	("hardware accelerator" and java) and oo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 19:39
4	31	("hardware accelerator" and java) and "object-oriented"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 19:40

Term used **java** Found **15** of **252 searched out of 252.**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 15 of 15

Relevance scale

1 Improving Java performance using hardware translation
Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John
June 2001 **Proceedings of the 15th international conference on Supercomputing**
Full text available: pdf(254.91 KB) Additional Information: full citation, abstract, references, citings, index terms

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

2 Virtual Java/FPGA interface for networked reconfiguration
Yajun Ha, Geert Vanmeerbeeck, Patrick Schaumont, Serge Vernalde, Marc Engels, Rudy Lauwereins, Hugo De Man
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Full text available: pdf(242.47 KB) Additional Information: full citation, abstract, references, index terms

A virtual interface between Java and FPGA for networked reconfiguration is presented. Through the Java/FPGA interface, Java applications can exploit hardware accelerators with FPGAs for both functional flexibility and performance acceleration. At the same time, the interface is platform independent. It enables the networked application developers to design their applications with only one interface in mind when considering the interfacing issues. The virtual interface is part of our work to ...

3 A survey of processors with explicit multithreading
Theo Ungerer, Borut Robič, Jurij Šilc
March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1
Full text available: pdf(920.16 KB) Additional Information: full citation, abstract, references, index terms

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors.A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

4 Attacking the semantic gap between application programming languages and configurable hardware

Greg Snider, Barry Shackleford, Richard J. Carter

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(258.65 KB) Additional Information: full citation, abstract, references, index terms

It is difficult to exploit the massive, fine-grained parallelism of configurable hardware with a conventional application programming language such as C, Pascal or Java. The difficulty arises from the mismatch between the synchronous, concurrent processing capability of the hardware and the expressiveness of the language-the so-called "semantic gap." We attack this problem by using a programming model matched to the hardware's capabilities that can be implemented in any (unmodified) objec ...

5 Architectures: 3D graphics LSI core for mobile phone "Z3D"

Masatoshi Kameyama, Yoshiyuki Kato, Hitoshi Fujimoto, Hiroyasu Negishi, Yukio Kodama, Yoshitsugu Inoue, Hiroyuki Kawai

July 2003 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware**

Full text available: pdf(649.83 KB) Additional Information: full citation, abstract, references

In this paper we describe the architecture of the 3D graphics LSI core for mobile phone "Z3D". The major 3D graphics applications on mobile phones are character animation and games. While a character animation or a game is running, the CPU has to be used for the communication to the center machine and CPU clock frequency is low. Therefore, the requirement of Z3D is small, low power, and CPU free. The pipeline of Z3D is composed of a geometry engine, rendering engine, and pixel engine. Generally, ...

Keywords: graphics accelerator, graphics hardware, rendering hardware

6 Industrial sessions: Web Services: Enabling sovereign information sharing using Web Services

Rakesh Agrawal, Dmitri Asonov, Ramakrishnan Srikant

June 2004 **Proceedings of the 2004 ACM SIGMOD international conference on Management of data**

Full text available: pdf(129.11 KB) Additional Information: full citation, abstract, references

Sovereign information sharing allows autonomous entities to compute queries across their databases in such a way that nothing apart from the result is revealed. We describe an implementation of this model using web services infrastructure. Each site participating in sovereign sharing offers a data service that allows database operations to be applied on the tables they own. Of particular interest is the provision for binary operations such as relational joins. Applications are developed by combi ...

7 DRM experience: Digital rights management in a 3G mobile phone and beyond

Thomas S. Messerges, Ezzat A. Dabbish

October 2003 **Proceedings of the 2003 ACM workshop on Digital rights management**

Full text available: pdf(306.59 KB) Additional Information: full citation, abstract, references, index terms

In this paper we examine how copyright protection of digital items can be securely managed in a 3G mobile phone and other devices. First, the basic concepts, strategies, and requirements for digital rights management are reviewed. Next, a framework for protecting digital content in the embedded environment of a mobile phone is proposed and the elements in this system are defined. The means to enforce security in this system are described and a novel "Family Domain" approach to content management ...

Keywords: MPEG-21, copyright protection, cryptography, digital content, digital rights management, embedded system, key management, mobile phone, open mobile alliance,

security

8 Security as a new dimension in embedded system design: Security as a new dimension in embedded system design

Srivaths Ravi, Paul Kocher, Ruby Lee, Gary McGraw, Anand Raghunathan

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(209.10 KB) Additional Information: full citation, abstract, references, index terms

The growing number of instances of breaches in information security in the last few years has created a compelling case for efforts towards secure electronic systems. Embedded systems, which will be ubiquitously used to capture, store, manipulate, and access data of a sensitive nature, pose several unique and interesting security challenges. Security has been the subject of intensive research in the areas of cryptography, computing, and networking. However, despite these efforts, *security is ...*

***Keywords**: PDAs, architectures, battery life, cryptography, design, design methodologies, digital rights management, embedded systems, performance, security, security processing, security protocols, sensors, software attacks, tamper resistance, trusted computing, viruses*

9 Design space exploration and architectural design of HW/SW systems: Hardware support for real-time embedded multiprocessor system-on-a-chip memory management

Mohamed Shalan, Vincent J. Mooney

May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**

Full text available: pdf(533.74 KB) Additional Information: full citation, abstract, references, index terms, review

The aggressive evolution of the semiconductor industry --- smaller process geometries, higher densities, and greater chip complexity --- has provided design engineers the means to create complex high-performance Systems-on-a-Chip (SoC) designs. Such SoC designs typically have more than one processor and huge memory, all on the same chip. Dealing with the global on- chip memory allocation/de-allocation in a dynamic yet deterministic way is an important issue for the upcoming billion transistor mu ...

Keywords: Atalanta, SoCDMMU, System-on-a-Chip, dynamic memory management, embedded systems, real-time operating systems., real-time systems, two-level memory management

10 DVS: An Object-Oriented Framework for Distributed Verilog Simulation

Lijun Li, Hai Huang, Carl Tropper

June 2003 **Proceedings of the seventeenth workshop on Parallel and distributed simulation**

Full text available: pdf(161.05 KB) Publisher Site Additional Information: full citation, abstract, index terms

There is a wide-spread usage of hardware design languages(HDL) to speed up the time-to-market for the designof modern digital systems. Verification engineers can simulatehardware in order to verify its performance and correctnesswith help of an HDL. However, simulation can'tkeep pace with the growth in size and complexity of circuitsand has become a bottleneck of the design process. DistributedHDL simulation on a cluster of workstations hasthe potential to provide a cost-effective solution to th ...

11 Articles: Blurring Lines Between Hardware and Software

Homayoun Shahri

April 2003 **Queue**, Volume 1 Issue 2

Full text available: html(23.93 KB) Additional Information: full citation, index terms

12 A hardware accelerator for the specular intensity of phong illumination model in 3-dimensional graphics

Young-Su Kwon, In-Cheol Park, Chong-Min Kyung

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(347.17 KB) Additional Information: full citation, references

13 Procedure based program compression

Darko Kirovski, Johnson Kin, William H. Mangione-Smith

December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.15 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Cost and power consumption are two of the most important design factors for many embedded systems, particularly consumer devices. Products such as personal digital assistants, pagers with integrated data services and smart phones have fixed performance requirements but unlimited appetites for reduced cost and increased battery life. Program compression is one technique that can be used to attack both of these problems. Compressed programs require less memory, thus reducing the cost of both direc ...

Keywords: RAM, battery life, cached procedures, communications applications, compressed memory, consumer devices, cost, design factors, directory structure, embedded systems, high-capacitance bus traffic, integrated data services, memory reduction, memory references, multimedia applications, pagers, performance requirements, personal digital assistants, power consumption, procedural reference resolution, procedure-based program compression, run-time performance overhead, smart telephones, source coding, transparent program compression

14 Tools: Automated tools to implement and test Internet systems in reconfigurable hardware

John W. Lockwood, Chris Neely, Chris Zuver, Dave Lim

July 2003 **ACM SIGCOMM Computer Communication Review**, Volume 33 Issue 3

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

Tools have been developed to automatically integrate and test networking systems in reconfigurable hardware. These tools dynamically generate circuits for Field Programmable Gate Arrays (FPGAs). A library of hardware-accelerated modules has been developed that processes Internet Protocol (IP) packets, performs header rule matching, scans pocket payloads, and implements per-flow queueing. Other functions can be added to the library as extensible modules.An integration tool was developed to enable ...

Keywords: Field Programmable Gate Array (FPGA), Internet, firewall, network intrusion detection and prevention, networks, reconfigurable hardware, tools

15 A Hardware/Software Reconfigurable Architecture for Adaptive Wireless Image Communication

Debashis Panigrahi, Clark N. Taylor, Sujit Dey

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(162.99 KB) Additional Information:

Publisher Site

full citation, abstract

With the projected significant growth in mobile internet and multimedia services, there is a strong demand for next-generation appliances capable of wireless image communication. One of the major bottlenecks in enabling wireless image communication is the high energy requirement, which may surpass the current and future capabilities of battery technologies. Past studies have shown that the bottlenecks can be overcome by developing adaptive multimedia compression algorithms which can adapt to dyn ...

Keywords: Adaptive, reconfigurable architecture, image compression, wireless multimedia

Results 1 - 15 of 15

Your search matched **2** of **1053485** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

hardware accelerator and java Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Virtual Java/FPGA interface for networked reconfiguration**
Yajun Ha; Vanmeerbeeck, G.; Schaumont, P.; Vemalde, S.; Engels, M.; Lauwereins, R.; De Man, H.;
Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. Asia and South Pacific , 30 Jan.-2 Feb. 2001
Pages:558 - 563

[Abstract] [PDF Full-Text (436 KB)] **IEEE CNF**

---

2 **Adaptive solid texturing for Web3D applications**
Bing-Yu Chen; Nishita, T.;
Computer Graphics and Applications, 2002. Proceedings. 10th Pacific Conference on , 9-11 Oct. 2002
Pages:433 - 434

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**
